IN THE SPECIFICATION:

Please add at page 1, line 1:

This national stage application claims the benefit of:

U.S. Provisional Application No. 60/184,192, filed on 22 February 2000, and entitled "*Method and Apparatus for Wafer and Device Level Testing for an RSL Logic Device*," and

U.S. Provisional Application No. 60/234,647, filed on 22 September 2000, and entitled "*Memory Tester Architecture.*"

Respectfully submitted,

Brian F. Russell

Brian F. Russell
Reg. No. 40,796
BRACEWELL & PATTERSON, L.L.P.
Suite 350 Lakewood on the Park
7600B North Capital of Texas Highway
Austin, Texas 78731-1168
Telephone: (512) 343-6116

ATTORNEY FOR APPLICANT